REMARKS

This is in response to the Office Action mailed on March 29, 2004.

Claims 1, 6, 13, 22, 31, 40, 47, 49, 79, and 82 are amended. Claims 1-49 and 74-84 are now pending in this application.

Applicant amends claims 1, 6, 13, 22, 31, 40, 47, 49, 79, and 82 for clarity. These claims are not amended in response to any substantive rejection.

Information Disclosure Statement

Applicant submitted an Information Disclosure Statement and a 1449 Form on April 2, 2004. Applicant respectfully requests that initialed copies of the 1449 Forms be returned to Applicants' Representatives to indicate that the cited references have been considered by the Examiner.

Reservation of the Right to Swear Behind References

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§112 Rejection of the Claims

Claims 1-29 and 79-84 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant respectfully traverses and asserts that these claims meet the requirements of §112, second paragraph. Applicant requests that the rejection be reconsidered and withdrawn. Applicant believes that claims 1-29 and 79-84 are now in condition for allowance.

§102 Rejection of the Claims

Claims 1-19, 21-27, 29-38, 40-47, 74 and 76-84 were rejected under 35 USC § 102(e) as being anticipated by Hassoun et al. (U.S. 6,587,534).

Hassoun discloses in FIG. 3 a controller 330 that receives a configuration signal CFG on line 308 and phase information from a phase detector 320. Hassoun also discloses in FIG. 3 a delayed clock signal D_CLK and a number of phase-shifted clock signals P_CLK_1 through P_CLK_N-1. Controller 330 of Hassoun provides select signals to output generator 340 to enable output generator 340 to select either the delayed clock signal D_CLK or one of the phase-shifted clock signals P_CLK_1 through P_CLK_N-1 as an output clock signal O_CLK. FIG. 3 of Hassoun does not show signal labels for the select signals from the output nodes of controller 330. However, in FIG. 8, Hassoun discloses that the select signals from controller 330 to output generator 340 are provided on select terminals 812.

Independent claim 41 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to enable the selector to replace the second delayed signal with the first delayed signal when the phase detect signal is activated and the command signal is not activated".

In rejecting claim 41, the Office Action compares output generator 340 of Hassoun to the selector of claim 41, controller 330 of Hassoun to the command react circuit of claim 41, the CFG signal of Hassoun to the command signal of claim 41, the phase information of Hassoun to the phase detect signal of claim 41, and the select signals from the output of controller 330 of Hassoun to the command set signal of claim 41.

Applicant uses the same comparison indicated in the Office Action when Applicant reviews the entire the disclosure of Hassoun to determine whether Hassoun discloses all of the elements recited in claim 41. However, Applicant is unable to find in Hassoun all of the elements recited in claim 41. For example, Applicant is unable to find in Hassoun that the select signals (the command set signal of claim 41) on output nodes of controller 330 (the command

react circuit of claim 41) enables output generator 304 (the selector of claim 41) to replace a first signal among the D_CLK, and P_CLK_1 through P_CLK_N-1 signals (the first delayed signal of claim 41) with a second signal among the D_CLK, and P_CLK_1 through P_CLK_N-1 signals (the second delayed signal of claim 41) when the CFG signal (the command signal of claim 41) is activated while the REF_CLK signal (the external clock signal of claim 41) and the first signal among the D_CLK, and P_CLK_1 through P_CLK_N-1 signals (the internal clock signal of claim 41) are synchronized. Further, Applicant is also unable to find in Hassoun that the select signals (the command set signal of claim 41) of controller 330 (the command react circuit of claim 41) enables output generator 304 (the selector of claim 41) to replace the second signal among the D_CLK, and P_CLK_1 through P_CLK_N-1 signals (the second delayed signal of claim 41) with the first signal among the D_CLK, and P_CLK_1 through P_CLK_N-1 (the first delayed signal of claim 41) when the phase information (phase detect signal of claim 41) is activated and the CFG signal (the command signal of claim 41) is not activated.

Based on the discussion above, since Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to enable the selector to replace the second delayed signal with the first delayed signal when the phase detect signal is activated and the command signal is not activated". Thus, claim 41 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 41 be reconsidered and withdrawn and that claim 41 and dependent claims of claim 41 be allowed.

Independent claim 1 recites, among other things, "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal". Applicant is unable to find in Hassoun "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal to provide the internal clock signal and for enabling the selector to select the first delayed

signal based on a second state of the command to provide the internal clock signal". Thus, claim 1 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 41 be reconsidered and withdrawn and that claim 41 and dependent claims of claim 41 be allowed.

Independent claim 6 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Thus, claim 6 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 6 be reconsidered and withdrawn and that claim 6 and dependent claims of claim 6 be allowed.

Independent claim 13 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first

delayed signal when the command signal is deactivated". Thus, claim 13 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 13 be reconsidered and withdrawn and that claim 13 and dependent claims of claim 13 be allowed.

Independent claim 22 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Thus, claim 22 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 22 be reconsidered and withdrawn and that claim 22 and dependent claims of claim 22 be allowed.

Independent claim 30 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized and to enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external

and internal clock signals are synchronized and to enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated". Thus, claim 30 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 30 be reconsidered and withdrawn and that claim 30 and dependent claims of claim 30 be allowed.

Independent claim 74 recites, among other things, "selecting a first delayed signal among the multiple delayed signals to generate an internal clock signal, synchronizing the internal and external clock signals, selecting a second delayed signal among the multiple delayed signals to generate the internal clock signal when a command signal is activated while the external and internal clock signals are synchronized, and reselecting the first delayed signal to generate the internal clock signal when the command signal is deactivated". Applicant is unable to find in Hassoun "selecting a first delayed signal among the multiple delayed signals to generate an internal clock signal, synchronizing the internal and external clock signals, selecting a second delayed signal among the multiple delayed signals to generate the internal clock signal when a command signal is activated while the external and internal clock signals are synchronized, and reselecting the first delayed signal to generate the internal clock signal when the command signal is deactivated". Thus, claim 74 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 74 be reconsidered and withdrawn and that claim 74 and dependent claims of claim 74 be allowed.

Independent claim 79 recites, among other things, "selecting a signal among the first and second delayed signals to generate an clock internal signal, adjusting the amount of delay until the external and internal clock signals are synchronized, reducing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism". Applicant is unable to find in Hassoun "selecting a signal among the first and second delayed signals to generate an clock internal signal, adjusting the amount of delay until the external and internal clock signals are synchronized, reducing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism". Thus, claim 79 is patentable over Hassoun. Accordingly, Applicant requests that

the rejection of claim 41 be reconsidered and withdrawn and that claim 41 and dependent claims of claim 41 be allowed.

Independent claim 82 recites, among other things, "selecting a signal among the first and second delayed signals to generate an clock internal signal, adjusting the amount of delay until the external and internal clock signals are synchronized, increasing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism". Applicant is unable to find in Hassoun "selecting a signal among the first and second delayed signals to generate an clock internal signal, adjusting the amount of delay until the external and internal clock signals are synchronized, increasing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism". Thus, claim 82 is patentable over Hassoun. Accordingly, Applicant requests that the rejection of claim 82 be reconsidered and withdrawn and that claim 82 and dependent claims of claim 82 be allowed.

§103 Rejection of the Claims

Claims 20, 28, 39, 48-49 and 75 were rejected under 35 USC § 103(a) as being unpatentable over Hassoun et al.

Applicant respectfully traverses. Claims 20, 28, 39, 48-49 and 75 are dependent claims of various independent claims above. Since the independent claims are patentable over Hassoun based on the discussion above regarding the independent claims, these dependent claims are also patentable over Hassoun because the independent claims are patentable over Hassoun. Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claims 20, 28, 39, 48-49 and 75 be allowed.

Nothwithstanding that the dependent claims 20, 28, 39, 48-49 and 75 claims are patentable because the independent claims are patentable, Applicant further traverses the rejection of the dependent claims under 35 USC § 103(a) because the Office Action does not provide documents to support the rejection.

In rejecting claims 20, 28, 39, 48-49 and 75, the Office Action indicates that

"It would have been obvious to one of ordinary skill in the art to implement circuitry to generate a phase lock signal, as indicated in claim 48, to indicate whenever the output clock signal is locked with the external clock input. Therefore, it would have been obvious to one of ordinary skill in the art to utilize that phase lock signal with the prior art in order to prevent the command react circuit inadvertently activated when those lock signals are not locked."

The portion of the Office Action above indicates that claims 20, 28, 39, 48-49 and 75 are obvious. However, the Office Action does not provides any documents to show that claims 20, 28, 39, 48-49 and 75 are obvious. Therefore, Applicant assumes that the Examiner is taking Official Notice in rejecting claims 20, 28, 39, 48-49 and 75. Applicant respectfully objects to the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the taking of Official Notice and requests that the Examiner provides documents to support the rejection of claims 20, 28, 39, 48-49 and 75. Absence of any document to support the rejection, Applicant requests that the rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28th day of July, 2004.

Amy Moriarty
Name

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Signature